

# Submicron Optical Microlithography Based On Interferometric Phase Shifting

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## ABSTRACT

One of the most critical processing steps in the fabrication of integrated circuits is microlithography. The design of high density DRAMs requires the accurate patterning of submicron structures. The manufacturability of VLSI components can be greatly improved through the integration of computer aided design and simulation software with an advanced interferometric optical system. In a new approach, a typical line and space pattern with features as fine as  $0.3 \mu\text{m}$  has been produced using a mask that has both transmitting areas and reflective areas and 355 nm laser illumination.

## 1. INTERFEROMETRIC PHASE SHIFTING TECHNIQUE

This paper reports progress on the simulation and experimental details of a novel phase shifting technique for microlithography based on interferometry.<sup>1</sup> The use of phase shifting is one of the most promising techniques<sup>2</sup> to enhance the capabilities of optical microlithography for the production of future generations of high density DRAMs. The design and production of special multi-layer dielectric masks containing phase shifting elements is a severe limitation of the current phase shifting mask technology.

Our new phase shifting mask technique is based upon a special interferometer, with a mask that has transmitting and reflective areas corresponding to the pattern design needed for the VLSI circuit. This new mask design is a single layer chrome mask which greatly simplifies the mask production process. The incoming laser beam is split into two. These beams irradiate the mask from both the front and back side via two beam splitters. The optical paths of the beams are chosen so that the phase of the two beams is different by an odd multiple of  $\pi$  radians at the surface of the mask by adjusting the position of the mask. This means that the electric fields of the reflected and transmitted beams have opposite signs and cancel each other when combined. The combined beams are projected onto the target wafer through a focusing lens which results in the phase shifted image of the pattern of the mask.

This new phase shifting method was confirmed experimentally using a frequency tripled Nd:YAG laser beam at 355 nm and UV photoresist. An SEM photograph of the line and space pattern is shown in Figure 1. Current research involves experiments with a 248 nm KrF laser illumination source which should yield a spatial resolution of  $0.2 \mu\text{m}$ .

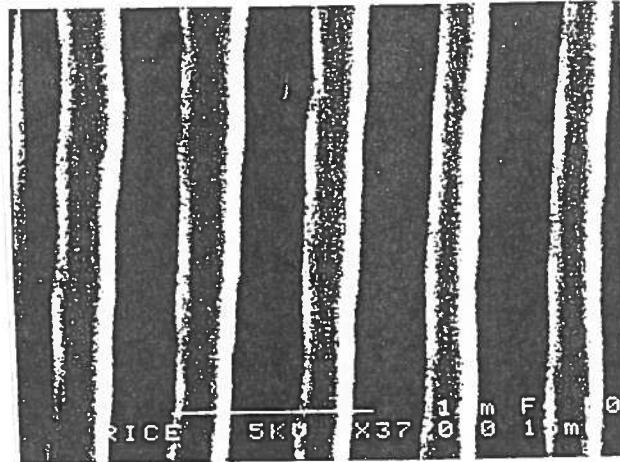


Figure 1: SEM Photograph on  $0.3 \mu\text{m}$  lines written in photoresist.

## 2. COMPUTER SIMULATION ENVIRONMENT

The lithography simulator, DEPICT, was used to evaluate the performance of this new scheme with various VLSI design patterns.<sup>3</sup> The simulations were used to evaluate the features of a related Integrated CAD Framework. This set of CAD tools links layout geometry editors, such as MAGIC, to lithographic simulators and provides expert information on the simulated optical and physical resolution of the feature to the designer. This will help designers to construct more compact circuits, as they will be able to see the effect on simulated manufactured silicon.

The algorithm followed by the current version of the Integrated CAD Framework contains several steps. Initially the layout geometry in CIF, GDS II, or MAGIC format is passed through a *filter* routine which identifies areas in the layout that are prone to problems arising out of photolithographic resolution tolerance. A corresponding input file for detailed analysis with process simulators, such as DEPICT, is created for these critical areas. An *analyzer* program then evaluates the simulator output (using pattern matching techniques) and determines whether the printed layout will match the designed mask for a particular set of process parameters. The *analyzer* program may also suggest modifications to the original layout which can then be updated based upon these corrections. This sequence of steps can then be repeated until the simulator and the VLSI designer agree that the layout is acceptable. This design environment was used to evaluate the geometry of the test mask built for the experiments for the new interferometric phase shifting method.

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### References

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