An Integrated CAD Framework Linking VLSI Layout Editors and Process Simulators

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ABSTRACT

As feature sizes in VLSI circuits extend into the far sub-micron range, new process techniques, such as using phase shifted masks for photolithography, will be needed. Under these conditions, the only means for the circuit designer to design compact and efficient circuits with good yield capabilities is to be able to see the effect of different design approaches on manufactured silicon, instead of solely relying on conservative general design rules. The Integrated CAD Framework accomplishes this by providing a link between a layout editor (Magic), advanced photolithographic techniques such as phase shifted masks, and a process simulator (Depict). This paper discusses some applications of this tool. A non-conventional process technique involving interferometric phase shifting and off-axis illumination has been evaluated using the tool. Also, a feature of the CAD Framework which allows representation of a phase shifted mask, together with its layout analysis capability has been used to compact a piece of layout by inserting phase shifted elements into it.

Keywords: Photolithographic simulations, critical features, CAD Framework.

1. INTRODUCTION

This paper presents some applications of the Integrated CAD Framework which provides a link between a layout editor (Magic[1]), advanced photolithographic techniques such as phase shifted masks, and a process simulator (Depict[2]). The Integrated CAD Framework identifies areas in the layout (in Magic, GDS-II or CIF format) that are more prone to problems arising out of photolithographic resolution tolerance, such as 'nested elbows' and 'open ends'. It uses Depict to provide the designer with a view of these areas after going through different process steps (such as, exposure and development of the resist coated wafer). It also compares the image of the mask after photolithographic simulation to the original mask, in order to determine acceptability of the design under the specified process conditions.

Such an evaluation provides a basis for making either process changes or pattern modifications which will cause the features to print accurately. Based on the analysis of the Integrated CAD Framework, the designer can make pattern modifications using techniques, such as optical proximity corrections (OPC[3]), which uses sub-resolution serifs and insets, to correct for effects such as corner rounding or linewidth non-uniformity. Thus the Integrated CAD Framework evaluates the effect of different design approaches on manufactured silicon, which will help circuit designers to design compact and efficient circuits with good yield capabilities.

Different application areas of such a CAD Framework have been studied. As described in Section 3 a pair of nested elbows have been evaluated under deep ultra violet lithography conditions. The evaluation of a non-conventional process technique involving interferometric phase shifting and off-axis illumination using the Integrated CAD Framework has been discussed in an earlier paper.[4] Section 4 presents an overview of this evaluation.

A feature of the CAD Framework which allows representation of a phase shifted mask, together with its layout evaluation capability, can be used to compact a piece of layout by inserting phase shifted elements into it. The insertion of phase shifted elements allows closer spacing between adjacent features than what is possible in a conventional transmission mask. The phase shifted elements are added to the layout and then the layout is evaluated by the Integrated CAD Framework (Section 5) to determine whether it can be accurately printed under specified process conditions.

2. FEATURES OF THE INTEGRATED CAD FRAMEWORK

2.1. Overview

The Integrated CAD Framework has two building blocks. The first block, the **filter**, identifies areas in the layout that are more prone to problems arising out of photolithographic resolution tolerance. It then provides the designer with a view of these areas after going through different process steps as specified by the user. The second block, the **analyzer**, analyzes the simulator outputs to determine whether the printed layout will match the designed mask as the process feature size is reduced.

The CAD Framework has been built as an extension to existing CAD tools, that is Magic and Depict. New modules have been added to Magic which identify problem areas in a layout database, translate the layout of these areas into a format understandable by Depict and analyze the output from Depict. An interface to these modules is provided as new commands to Magic.

2.2. Critical areas in masks

There are several typical patterns found in VLSI masks, each of which respond differently to scaling. However, some of the features (critical areas), such as 'elbows', 'open ends' and 'contact holes',[5] are found to be more prone to problems arising out of photolithographic resolution tolerance. In the case of 'nested elbows', as the linewidth decreases, the elbows tend to become rounded and there is bloating at the corners. Hence, if there are two elbows close to each other, there may be a short circuit near the corners. In the case of 'open ends', the ends tend to shrink and there is a shortening in line length. Currently, Depict cannot handle a large layout in a single simulation run. Also as the layout area to be simulated increases, the simulation time increases by a large amount. Thus, the Integrated CAD Framework detects the critical areas from a larger layout, and prepares the input for Depict for these areas only, instead of the whole layout. In addition to this, the Integrated CAD Framework marks the critical areas with appropriate labels based on the name of the cell and the co-ordinates of the critical area. Figure 1 shows the detection and labeling of elbows and open ends in a small piece of layout.
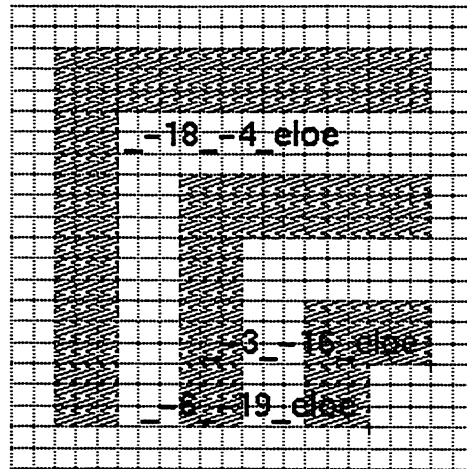
Figure 1: Some critical areas found by the Filter. (It should be noted that there are more than three critical areas found in this piece of layout. The additional areas have not been labeled in this figure in order to keep the figure readable.)

2.3. Process simulation

There are several process simulators available, each of which model different parts of the integrated circuit fabrication process. SPLAT,[6] SAMPLE-3D,[7] PROLITH,[8] FAIM,[9] and Depict are some of the commonly used optical projection lithography simulators. The Integrated CAD Framework uses Depict, which belongs to a suite of process simulators from Technology Modeling Associates.

2.4. Analysis of the simulation output

The Integrated CAD Framework analyzes the simulator output to determine an acceptance criteria for the mask considering the specified set of process parameters. It uses Depict to calculate the aerial intensity image of the mask and also to simulate exposure and development of the photoresist. The Integrated CAD Framework compares the image of the mask after photolithographic simulation to the original mask using pattern matching techniques.[10]

3. EVALUATION OF A SET OF ELBOWS UNDER DUV CONDITIONS

In this section, a pair of nested elbows, extracted from a larger layout, is evaluated under deep ultra violet (DUV) lithography conditions for linewidth ranging from 0.37μ to 0.25μ. The 'nested elbows' are extracted from a larger test layout. The modeling of the photoresist (SNR248 from Shipley Co.) as well as the exposure and development of the resist is done explicitly using data obtained from two papers,[11,12] in which, the performance of SNR248 photoresist is evaluated for different values of numerical aperture, defocus, exposure dose, resist thickness, softbake and post exposure bake, for a nominal linewidth of 0.35μ. The optical characteristics of silicon, the SNR248 resist, and a anti-reflective coating, as a function of wavelength ($248nm$) were specified to Depict. Also, a model for development of SNR248 based on the Mack model[13] was defined.

The evaluation of the structure for two different linewidths are shown in Figures 2 and 3. Figure 2.a shows the 2-D aerial intensity image and Figure 2.b the 1-D aerial intensity image calculated by Depict for a linewidth of 0.375 μm. Figure 2.c shows the exposed and developed structure with a cleared line in the center. The width of this cleared photoresist is used with the 1-D aerial intensity image of Figure 2.b to find the minimum intensity over the cleared line ('threshold intensity'). The 'threshold intensity' is reported below Figure 2.c. The 'threshold intensity' is applied to Figure 2.a to obtain the binary aerial intensity image in Figure 2.d, which is compared to the original mask in Figure 2.e to determine the 'match percentage'. The 'match percentage' is reported at the bottom of Figure 2. This analysis pronounces this layout with a linewidth of 0.375μm under the given process conditions a 'pass'.

Figure 3 shows a similar analysis for a linewidth of 0.24μm. However, in this case the analysis concludes that under the given process conditions, a pair of nested elbows with a linewidth of 0.24μm, cannot be printed accurately. Hence the analyzer marks it as a 'fail'. Table 1 summarizes the results of this experiment.

Linewidth(μ)	Match(%)	Result
0.37	87.5	PASS
0.30	73.6	FAIL
0.24	19.6	FAIL

Table 1: Results of the evaluation of elbows under DUV conditions

4. INTERFEROMETRIC PHASE SHIFTING AND OFF-AXIS ILLUMINATION

A non-conventional lithography technique combining off-axis illumination (OAI) with interferometric phase shifting (IPS),[14] developed at Rice University, has been reported in[4] an earlier paper. This paper also discussed the evaluation of a small layout containing a lines-and-spaces pattern using the Framework. The non-conventional lithography process was modeled using Depict and Magic.

The off-axis illumination was modeled in Depict by defining a new exposure machine. The illumination system has a pole whose center is 0.85 units away from the origin of the source co-ordinate system, the pole radius is 0.0125 units and the angular co-ordinate of the center of the pole with respect to the x-axis of the source co-ordinate system is -180°. In order to simulate the interferometric phase shifting effect, Magic was used to draw a phase shifted mask. The mask has two types of materials, one with a transmission amplitude of 1 and phase of 0° and the other with a transmission amplitude of 0.222 and a phase of 180°. The linewidth was 0.4μm and it was printed using a wavelength of 435.8nm on AZ1350J photoresist. The optical co-efficients used for AZ1350J were taken from the Depict library. The analysis results agreed closely with the experimental results.[4]
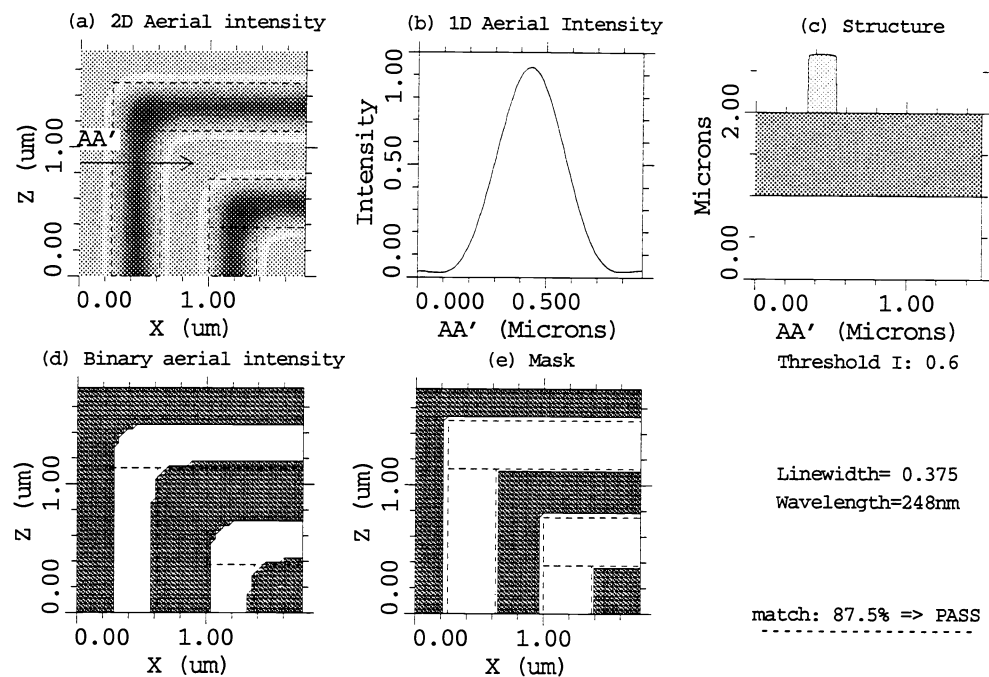
(a) 2D Aerial intensity

(b) 1D Aerial Intensity

(c) Structure

Threshold I: 0.6

(d) Binary aerial intensity

(e) Mask

Linewidth= 0.375
Wavelength=248nm

match: 87.5% => PASS

Figure 2: Output from the analyzer for $linewidth = 0.375\mu$

(a) 2D Aerial intensity

(b) 1D Aerial Intensity

(c) Structure

Threshold I: 0.6

(d) Binary aerial intensity

(e) Mask

Linewidth= 0.24
Wavelength=248nm

match: 19.6% => FAIL
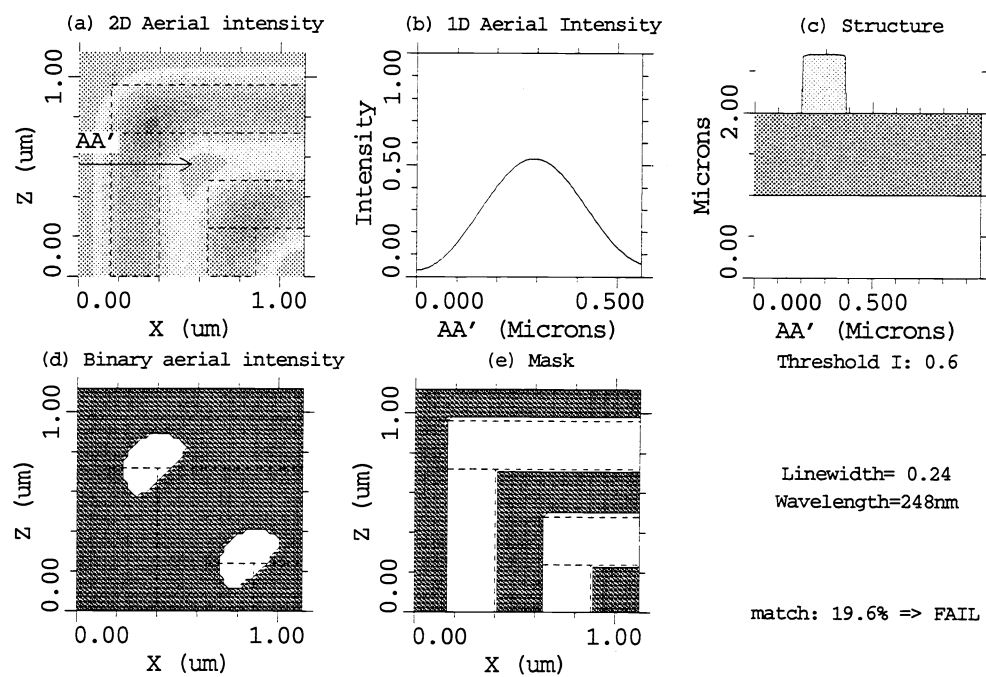
Figure 3: Output from the analyzer for $linewidth = 0.24\mu$

5. COMPACTION OF A LAYOUT USING PHASE SHIFTING

The feature of the CAD Framework which allows representation of a phase shifted mask, together with the analyzer was used to compact a piece of layout by inserting phase shifted elements into it. The piece of layout, evaluated in this section was taken from a larger design. This layout was generated automatically by a router in the Lager suite of CAD software.[15] The wire routing occurs between rows of standard cells that can be used to construct functional units such as adders or multipliers. The wire routing between the standard cells is done using two metal layers (metal1 and metal2 in Magic). Metal1 is run in the horizontal direction and metal2 is run in the vertical direction with appropriate contacts between the two layers. The piece of layout (Figure 4) extracted for this example, is a part of the metal1 layer of the wire routing. This layout has been already optimized by the router to have lines and spaces of width best suited for a transmission mask. This layout was taken and phase shifted parts were added to it with the assumption that phase shifting will allow closer spacing between the lines.[16] The compacted layout with and without the phase shifted portions was simulated using Depict and then evaluated by the Analyzer.

Such a compaction can be done based on the algorithm PSMGEN,[17] in which, a mono-layer layout file is converted to a phase shifted mask layout with minimum spacing between adjacent features as well as between a feature and a phase transition.

The compacted layout with and without the phase shifted elements were evaluated by the Analyzer. The process simulation parameters were obtained from the default Depict library. The photoresist used was KODAK820 and the aerial intensity image was obtained with light of wavelength 365 nm (i-line) and a lens of numerical aperture of 0.4. Figure 5 shows the binary aerial intensity image with an intensity threshold of 0.4, for the compacted layout without the phase shifted elements. The poor quality of the binary aerial intensity image clearly shows that the compacted layout cannot be used as a transmission mask. Figure 6 shows the binary aerial intensity image with an intensity threshold of 0.4, for the compacted layout with the phase shifted elements. The binary aerial intensity image closely resembles the mask and the Analyzer marks it as a 'pass'.

Thus, Figures 4-6 show that when a transmission mask is used, we cannot have compaction beyond the original layout. However, if we use phase shifting, we can have a smaller layout. This idea can be extended to build an automatic phase shift mask generator from a mono-layer layout. In this section, phase shifted elements were inserted in a relatively small piece of layout. The same technique can be automated and applied to larger layouts, such as high density DRAMs, in order to achieve larger percentages of compaction.

6. CONCLUSIONS

Some applications of the Integrated CAD Framework which links layout editors to process simulators has been presented. A wide range of processing techniques, such as phase shifting masks and off-axis illumination, can be modeled and evaluated using this system. Thus, the Integrated CAD Framework provides a good method of evaluating a layout or a process technique.
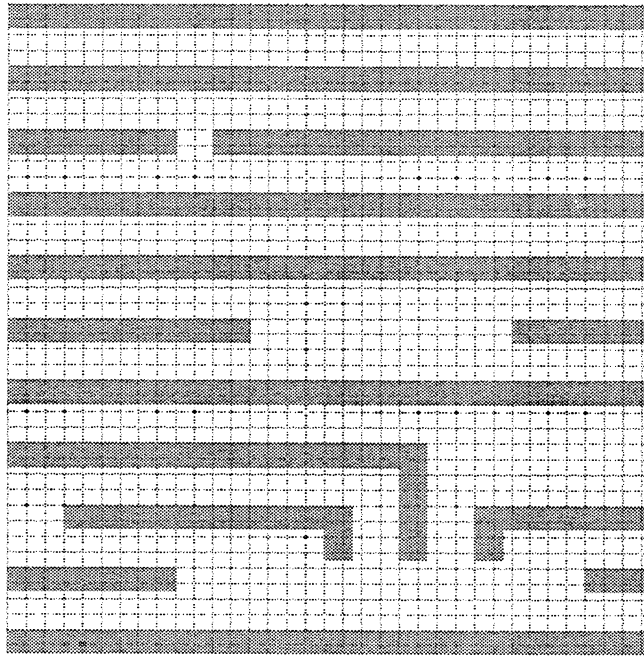
Figure 4: The original layout: Area: $10.37\mu m \times 8.62\mu m$, Linewidth: $0.75\mu m$
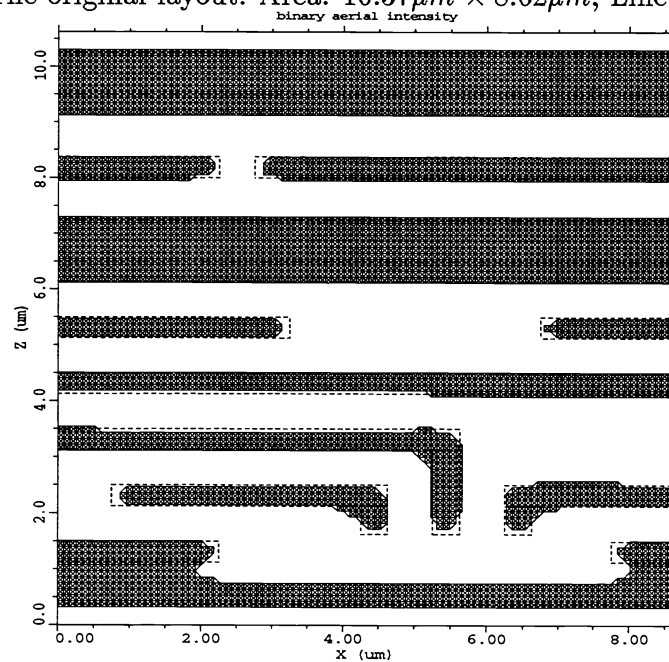

Figure 5: Binary aerial intensity image for the compacted layout without phase shifted elements: Area: $10.37\mu m \times 8.62\mu m$, Threshold: 0.4, Match: 80% => $FAIL$
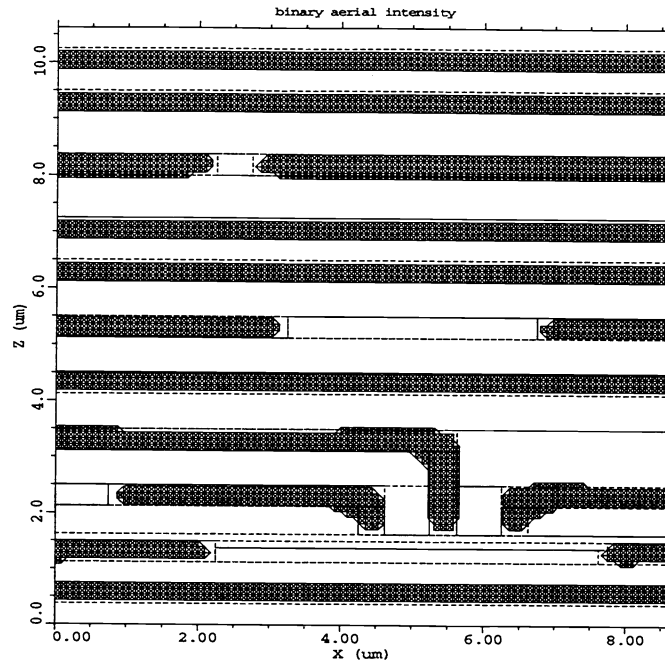
Figure 6: Binary aerial intensity image for the same compacted layout with phase shifting: Threshold: 0.4, Match: 90% => *PASS*

7. ACKNOWLEDGEMENTS

8. REFERENCES

[1] G. S. Taylor, J. K. Ousterhout, G. T. Hamachi, R. N. Mayo, and W. S. Scott. Magic: A VLSI layout system. *Proceedings of 21st IEEE/ACM Design Automation Conference*, pages 152–159, 1984.

[2] R. C. Pack and D. A. Bernard. DEPICT-2 applications for VLSI technology. *Technical Report, Technology Modelling Associates Inc.*, 1990. Palo Alto, CA.

[3] O. W. Otto and R. C. Henderson. Integrating proximity effects corrections with photomask data preparation. *Proceedings of SPIE - Optical/Laser Microlithography VIII*, pages 184–191, 1995.

[4] M. Erdélyi, C. Sengupta, Z. Bor, J. R. Cavallaro, M. Kido, M. C. Smayling, F. K. Tittel, W. L. Wilson, and G. Szabó. A new interferometric phase-shifting technique for sub-half-micron laser microlithography. *Proceedings of SPIE - Optical/Laser Microlithography VIII*, pages 827–837, 1995.

[5] D. M. Newmark and A. R. Neureuther. Phase-shifting mask design tool. *Proceedings of SPIE, 11th Annual BACUS Symposium on Photomask Technology*, 1604:226–235, 1991.

[6] K. K. H. Toh, D. Newmark, P. Flanner, D. Lee, M. Yeung, and A. R. Neureuther. *SPLAT v4.2 User's Guide*. EECS Dept, University of California, Berkeley, CA, December 1993.

[7] K. K. H. Toh and A. R. Neureuther. Three dimensional simulation of optical lithography. *Proceedings of SPIE - Optical/laser microlithography IV*, 1463:356–367, 1991.

[8] O. D. Crisalle, S. R. Keifling, D. E. Seborg, and D. A. Mellichamp. A comparision of the optical projection lithography simulators in SAMPLE and PROLITH. *IEEE Transactions on Semiconductor Manufacturing*, 5(1):14–26, February 1992.

[9] E. Barouch, U. Hollerbach, and R. Vallishayee. OPTIMASK: An OPC algorithm for chrome and phase-shift mask design. *Proceedings of SPIE - Optical/Laser Microlithography VIII*, pages 192–206, 1995.

[10] B. Dom, W. E. Blanz, C. Cox, D. Steele, and A. Dorundo. The segmentation engine: A real-time image-segmentation subsystem. *Proceedings of SPIE - Machine Vision Applications in Industrial Inspection II*, 2183:22–36, 1994.

[11] T. Ohfuji, O. Nalamasu, and D. R. Stone. Advanced dynamic process simulation for an excimer laser lithography. *J. Vac. Sci. Technol.*, B 11(6):2714–2719, Nov/Dec 1993.

[12] N. Samarakone, V. V. Driessche, P. Jaenen, L. Van den hove, D. Ritchie, and P. Luehrmann. Improving the performance and usability of a wet developable DUV resist, for sub - 500nm lithography. *Proceedings of SPIE - Optical/Laser Microlithography IV*, 1463:16–29, 1991.

[13] C. A. Mack. Development of positive photoresists. *J. Electrochem. Soc.*, 134(1):148–152, January 1987.

[14] M. Kido, G. Szabó, J. R. Cavallaro, W. L. Wilson, M. C. Smayling, and F. K. Tittel. Sub-micron optical lithography based on a new interferometric phase shifting technique. *Jpn. J. Appl. Phys.*, 34(8A):4269–4273, August 1995.

[15] C. B. Shung, R. Jain, K. Rimey, E. Wang, M. B. Srivastava, B. C. Richards, E. Lettang, S. K. Azim, L. Thon, P. N. Hilfinger, J. M. Rabaey, and R. W. Brodersen. An integrated CAD system for algorithm-specific IC design. *IEEE Transactions on Computer Aided Design*, 10(4):447–463, April 1991.

[16] K. Ooi, K. Koyama, and M. Kiryu. Method of designing phase-shifting masks utilizing a compactor. *Japanese Journal of Applied Physics*, 33:6774–6778, 1994.

[17] G. Galan, F. Lalanne, P. Schiavone, and J. Temerson. Application of alternating-type phase shift mask to polysilicon level for random logic circuits. *Japanese Journal of Applied Physics*, 33(12B):6779–6784, December 1994.