Automated Evaluation of Critical Features in VLSI Layouts Based on Photolithographic Simulations

Joseph R. Cavallaro, Chaitali Sengupta, Frank K. Tittel, William L. Wilson, Jr.
Rice University

ABSTRACT

This paper describes a CAD tool (An Integrated CAD Framework) which links VLSI layout editors to lithographic simulators and provides information on the simulated resolution of a feature to the circuit designer. The designer can modify the original layout based upon this analysis to create compact circuits with better yield capabilities. The objective of this project is to improve the manufacturability of high density VLSI intergrated circuits.

1. INTRODUCTION

At present, in a VLSI circuit design and fabrication process, the design phase and the process phase are completely isolated. Circuit designers are given a set of design rules, and a technology file in order to do their work. These design rules are based on a particular technology (process) and determine the minimum size and spacing of all layers of the circuit geometry in an attempt to maximize yield, performance and reliability. The design rules are optimized to give a good general layout from a single set of rules, but might not give the most optimum design in all cases.

As feature sizes become smaller (sub-micron range) and as the chip area becomes larger, new process techniques (such as, using phase shifted masks for photolithography), will be needed. Under these conditions, the only means for the circuit designer to design compact and efficient circuits with good yield capabilities is to be able to also see the effect of a particular layout on manufactured silicon. This can be accomplished by integrating process simulators with the layout editor that the circuit designer uses. Based on the information provided by the process simulators regarding the optical and physical resolution of the feature, the designer can alter the design rules in order to create better circuits.

2. INTEGRATED CAD FRAMEWORK

This paper overviews the design and implementation of the Integrated CAD Framework which integrates the design and process phases of IC fabrication by providing a link between a layout editor (Magic) and a process simulator (Depict, from Technology Modeling Associates). The Integrated CAD Framework uses a modified version of Magic's design rule checker to identify areas in the layout (in Magic, GDS-II or CIF format), such as 'nested elbows' (Fig. 1) and 'open ends', that are more prone to problems arising out of photolithographic resolution tolerance. It then automatically invokes Depict to provide the designer with a view of these areas after going through different process steps (such as, exposure and development of the resist coated wafer). The Integrated CAD Framework also compares the image of the mask after photolithographic simulation to the original mask using pattern matching techniques. It uses a 'degree of match' between these to determine acceptability of the mask under the specified process conditions. The designer can modify the layout based upon this analysis. An interface to all these capabilities is provided as new commands to Magic.

The Framework has been used to evaluate layouts for various process techniques, including a non-conventional technique involving interferometric phase shifting and off-axis illumination.[1] These evaluations illustrate the use of the Framework in analyzing a layout under specified process conditions as well as determining the limits of any lithographic process.[2]

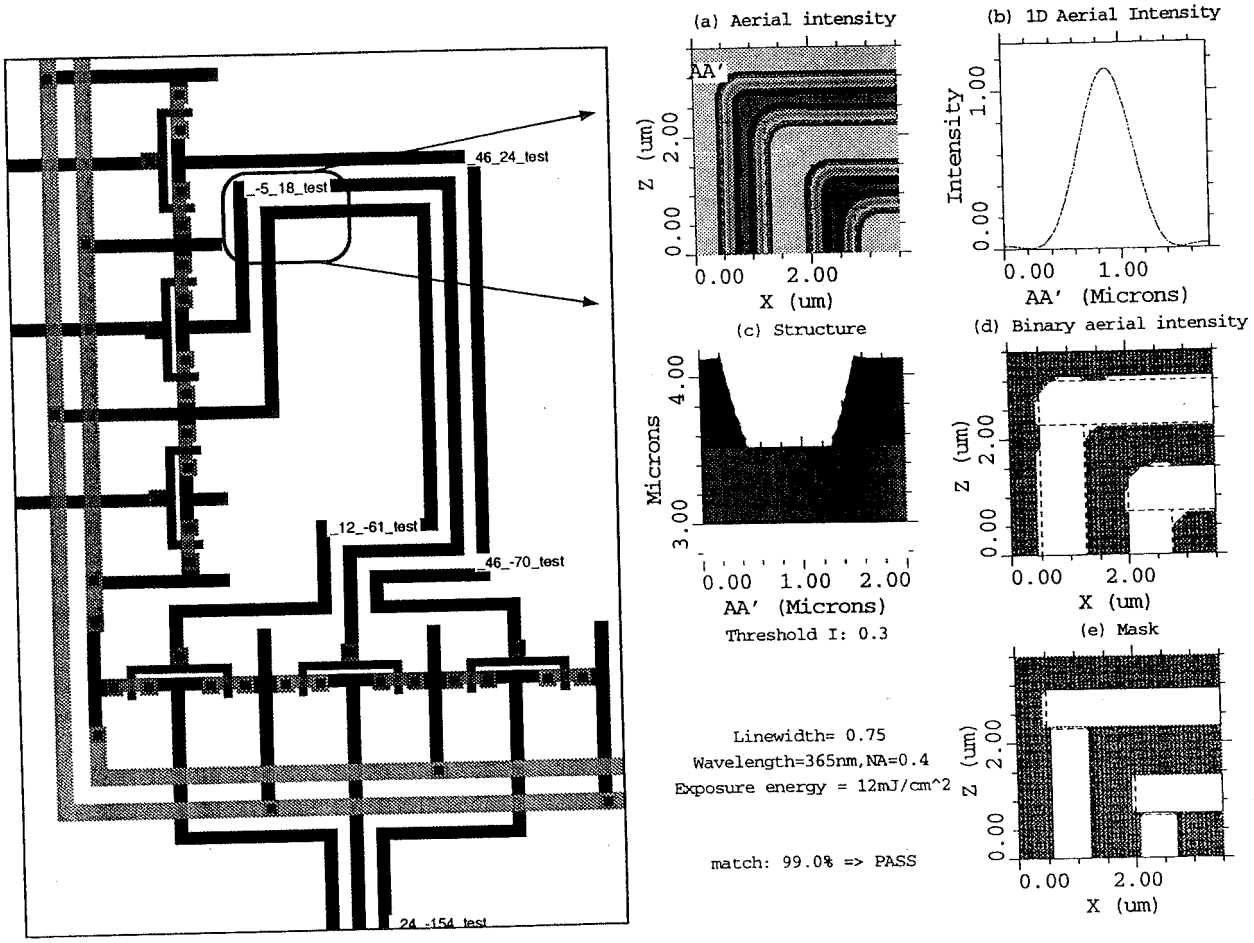

Figure 1: A layout evaluated by the Framework. The system detects the nested elbows and open ends and marks these with labels. Evaluation of the nested elbows for $linewidth = 0.75\mu m$

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References

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[2] C. Sengupta. An Integrated CAD Framework linking VLSI layout editors and process simulators. *M. S. Thesis, Rice University, Houston, TX*, 1995. Also available as ECE Technical Report #9501, Rice University, Houston, TX.