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Enhanced VLSI Manufacturability Using an Integrated CAD Framework

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ABSTRACT

Continued improvements in VLSI performance, circuit density and production costs are possible, in part, to significant advances in lithography. As feature sizes get smaller, design houses are faced with either improving the resolution of their optical lithography lines, or step-up to the cost of the newer x-ray based machines. The work at Rice University proposes to integrate design and process-specific CAD tools to provide further use of optical lithography equipment, while reducing feature sizes to improve manufacturability. By integrating photolithography simulators to layout editors, and by providing expert information on the simulated optical and physical resolution of the feature to the designer, compact and smaller circuits can be designed, which are governed by local design rules. This work is complemented by the development of a novel phase shifting technique at Rice based on interferometry which allows for the manufacture of features with high contrast and reduced feature size.

1. INTRODUCTION

Circuit designers are normally given a set of design rules, and a technology file in order to do their work. This isolates the designer from the process and manufacturing engineers, but at the same time limits the ability to push the technological barriers. As performance and yield of integrated circuits is more important, and assuming that the basic manufacturing lines are to remain at the current level of performance, the only means for the circuit designer to reduce feature sizes is to be able to also see its effect on manufactured silicon. This is accomplished by integrating photolithography simulators into the CAD framework that the circuit designer uses. A layout editor simply creates in graphical form the different masks needed by the manufacturing line; these days, there is emphasis on using phase-shifted masks as a means to further reduce feature size while maintaining the same contrast levels, and using the same equipment. The use of these phase-shifted masks also needs to be integrated into the circuit designer's framework, so that its effects can be simulated.

Design rules now become a guideline; they will be altered by the designer where possible, in order to create better circuits. At the same time, the engineer will know that by evaluating the desired transistor feature size and the processing line to be used, this enhanced CAD framework will allow determining the feasibility to manufacture, and a predicted yield. It will also be possible to determine if the target goals can not be attained with the proposed design and processing parameters used, at which time the additional tools would be able to correct for deficiencies, and present an alternate solution, for the design engineer to consider.

2. DESIGN TOOLS AVAILABLE TO THE ENGINEER

Circuit designers have access to different layout editors; for the purposes of this work, we have chosen to use Magic [2], and the CIF standardized output format. Integrated circuit process engineers also have several simulation tools; we have emphasized work on Depict-2 [3], and SPLAT v4.2 [4], as part of SAMPLE. The Magic layout editor has the capability to select parts of a layout, and extract a CIF file with its geometric description. An integrated CAD Framework would then use this generic file to analyze its physical properties with the aid of Depict-2 or SPLAT.

Results would be analyzed and reported back as a modified input file to the Magic session. Thus, the circuit designer would be able to, in an interactive manner, see the results of the changes done with the layout editor.

3. A GENERIC INTERFACE TO LAYOUT EDITORS

The first link between circuit designers and process engineers is to allow for the two sets of CAD tools to interact with each other. We have developed an initial filter program which uses as input the CIF files, and generates a command file for Depict-2. The program has been created in CLIPS, an expert systems programming tool, so that a set of rules can be used to determine the type of analysis to be performed, and to be able to correctly interpret the different results that will be obtained.

There have been other attempts to link layout editors to lithography simulators, the most notable being the work by Newmark [1], who describes the development of MASC, which "assists layout designers in deciding upon design rules, and determining the printability of a particular mask level." With the MASC tool, the circuit designer must manually analyze the simulation results and decide on a strategy to improve resolution. The current work at Rice University emphasizes on creating a closed-loop environment where the user does not need to learn about process engineering.

4. A SMART PHOTOLITHOGRAPHY EVALUATION TOOL

An important link in this CAD Framework is the means to provide an accurate and informed result of the attempts by the circuit designer to minimize the size of the circuits that are under development. This analyzer, currently under investigation by the authors, is an expert system based tool that has a database of knowledge in the photolithography, optics, and process engineering areas. It analyzes the results from the simulators, and interprets them to determine whether the feature is manufacturable, and whether its yield and resolution are acceptable. The circuit designer's goal will be to scale custom or cell-based circuits to the smallest manufacturable feature. This can be achieved:

- By using transmission and phase shifted masks at the time of manufacture,
- By analyzing *critical* geometries to investigate the limits of scaling and resolution,
- By modifying either standard cells and/or custom designs so that *critical* geometries can be scaled further.

At each step, the designer will be able to command an analysis of the modified feature, and, in an interactive fashion, be able to refine solutions at will. Figure 1 shows a system level block diagram of the complete CAD Framework. Shaded areas are the links that need to be created in order to have an integrated environment.

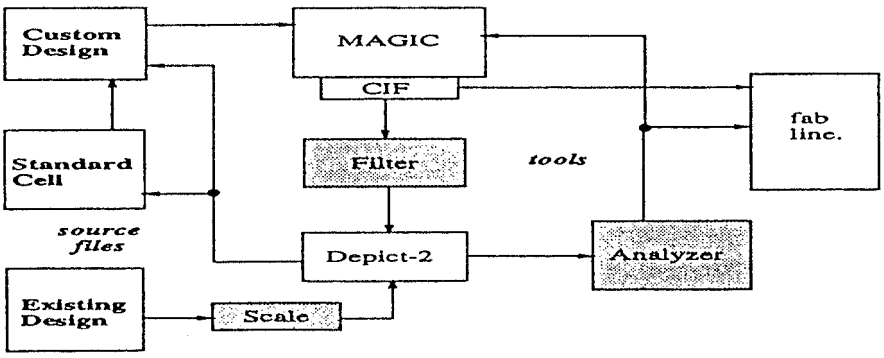

Figure 1: System Level Block Diagram of the CAD Framework

Acknowledgments

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