Automated Evaluation of Critical Features in VLSI Layouts Based on Photolithographic Simulations

Chaitali Sengupta, *Student Member, IEEE*, Joseph R. Cavallaro, *Member, IEEE*, William L. Wilson, Jr., *Senior Member, IEEE*, and Frank K. Tittel, *Fellow, IEEE*

***Abstract*—In this paper, we address the problem of identifying and evaluating "critical features" in an integrated circuit (IC) layout. The "critical features" (e.g., nested elbows and open ends) are areas in the layout that are more prone to defects during photolithography. As feature sizes become smaller (sub-micron range) and as the chip area becomes larger, new process techniques (such as, using phase shifted masks for photolithography), are being used. Under these conditions, the only means to design compact circuits with good yield capabilities is to bring the design and process phases of IC manufacturing closer. This can be accomplished by integrating photolithography simulators with layout editors. However, evaluation of a large layout using a photolithography simulator is time consuming and often unnecessary. A much faster and efficient method would be to have a means of automatically identifying "critical features" in a layout and then evaluate the "critical features" using a photolithography simulator. Our technique has potential for use either to evaluate the limits of any new and nonconventional process technique in an early process definition phase or in a mask house, as a postprocessor to improve the printing capability of a given mask. This paper presents a CAD tool (An Integrated CAD Framework) which is built upon the layout editor, Magic, and the process simulator, Depict 3.0, that automatically identifies and evaluates "critical features."**

***Index Terms*—Critical features, photolithography, process simulation.**

I. Introduction

A LARGE part of the phenomenal growth in semiconductor productivity in recent years has been the result of lithography improvements: smaller feature sizes, tighter overlay and higher density chips [1]. As feature sizes become smaller (sub-micron range) and as the circuits become larger, new photolithography techniques (such as, using phase shifted masks [2], [3]), are being used. Under these conditions, if designers or process engineers are able to see the effects of certain layout features on manufactured silicon, they can better exploit the advantages provided by these new process techniques in terms of minimized printed linewidth.

Traditionally, in a VLSI circuit design and fabrication process, the design phase and the process phase are completely isolated. Circuit designers are given a set of design rules, based on which they generate a layout. These design rules are based on a particular technology (process) and determine the minimum size and spacing of all layers of the circuit geometry in an attempt to maximize yield, performance and reliability. The design rules are optimized to give a good general layout from a single set of rules, but are conservative and might not give the most optimum design in all cases. However, to design and fabricate compact circuits with good yield capabilities, designers or process engineers need to see the effects of certain layout features on manufactured silicon. This may be achieved by bringing the design and process phases closer. For this reason, there is a current interest in industry, as shown by the series of workshops sponsored by SEMATECH [4], to explore the issues regarding integration of these two phases.

Such an integration can be accomplished by integrating process simulators with layout editors. When process simulators are integrated with layout editors, design rules will become only a guideline. Based on the expert information provided by the process simulators regarding the optical and physical resolution of the feature, the design rules may be altered where possible, in order to create more compact and faster circuits. Such, a technique may be used in the mask house, as a postprocessor to improve the printing capability of a given mask, especially, for applications like DRAM cells. In DRAM cell design, achieving a high level of compaction is imperative and hence, fine tuning of the layout through a closer interface of the design to the process phase is worthwhile.

On the other hand, an integration of process simulators with layout editors can also be used to evaluate the limits of any new and nonconventional process technique, in the early process definition phase. The process simulator will model the new process techniques and various layout features can be evaluated under these new process conditions.

A. Overview of the Integrated CAD Framework

This paper presents the design and implementation (Section II) of the Integrated CAD Framework [5] which integrates the design and process phases of IC fabrication by providing a link between a layout editor (Magic [6]), techniques (such as, using phase shifted masks for photolithography), and a process simulator (Depict 3.0 from Technology Modeling Associates [7]). The Integrated CAD Framework uses a modified version of Magic's design rule checker to identify "critical features" in the layout that are more prone to defects due to the photolithographic process. It then automatically invokes Depict to provide a view of

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The authors are with the Electrical and Computer Engineering Department, Rice University, Houston, TX 77005-1892 USA (e-mail: chaitali@rice.edu; cavallar@rice.edu; wlw@rice.edu; fkt@rice.edu).

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these areas after going through different process steps as specified by the user (such as, exposure and development of the resist coated wafer). Next, it compares the image of the mask after photolithographic simulation to the original mask using pattern matching techniques. It uses a "degree of match" between these to determine acceptability of the mask under the specified process conditions. The layout may be modified based upon this analysis.

The CAD Framework has been built as an extension to existing CAD tools, that is Magic and Depict 3.0. New modules have been added to Magic which identify "critical features" in a layout database, translate the layout of these areas into a format understandable by Depict, and analyze the output of Depict. An interface to these modules is provided as new commands to Magic.

It should be noted that the Integrated CAD Framework has been built using Magic and Depict 3.0 in order to illustrate the techniques developed to identify and evaluate the "critical features." However, the same techniques can also be implemented using other layout editors or process simulators.

Different application areas of such a CAD Framework have been studied and the results are presented in Section III.

B. Issues Related to the Design of the Integrated CAD Framework

1) Critical Features in Masks: The "critical area" of a semiconductor device has been defined in literature [8], [9] as "the portion of the active area that is susceptible to defects, i.e., the area within which the ocuurrence of a defect results in yield loss." Now, the defects arising from the lithography process may be broadly classified as point defects or line registration errors [10]. Point defects are caused by opaque particles gathered on the surface of the mask or by transparent spots in the opaque regions of the mask. These defects depend on the environment of the mask shop and is not a function of the process parameters. A line registration error is the error in the location of the edge of various regions in the IC structure and is dependent on various process parameters such as, wavelength, numerical aperture of the lens, exposure dose, resist thickness, and others. Different features in the layout will respond differently to different values of all these parameters.

In the context of this paper, "critical features" refer to certain geometries in the layout (such as, "nested elbows," and "open ends"), which, when printed using specified lithographic techniques, will cause a line registration error greater than a certain acceptable limit (10% in the implementation described in this paper). Such line registration errors, can cause a short circuit or a break which in turn results in yield loss. Similarly, "printability" refers to the ability of a specific process to print a certain "critical feature" without causing any line registration errors.

The idea of "critical features" is distinct from the definition of "critical areas" in [8], [9]. "Critical features" are circuit geometries that are susceptible to defects (line registration errors) during lithography. On the other hand, the area of the layout within which the occurrence of such a defect, makes it a fault, is a "critical area"—where, a fault is a defect which causes yield loss.

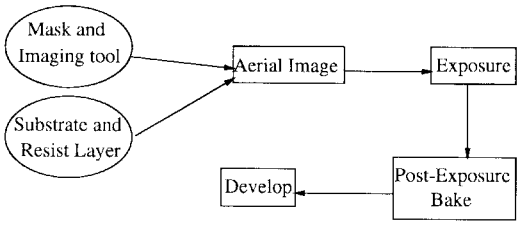

Fig. 1. Typical lithography simulation flow.

There are several "critical features" that can be found in VLSI masks, each of which respond differently to scaling. Some typical examples of critical features are—"nested elbows," "open ends," "closely spaced parallel lines" and "arrays of contact holes," [11]. In the case of "nested elbows," as the linewidth decreases, the elbows tend to become rounded and there is bloating at the corners. This effect can be seen in Figs. 10 and 11. Hence, if there are two elbows close to each other, there may be a short circuit near the corners. This effect has also been discussed in [12]. In the case of "open ends," the ends tend to shrink and there is a shortening in line length. This effect has been demonstrated in [13]. It arises due to finite bandwidth effects of various lithographic systems which causes the so-called corner-rounding and if the corners are close enough as in "open ends," line shortening. In [13], the authors have developed an extended Hopkins-based model that analytically predicts the line shortening error based on knowledge of the mask and process parameters.

Many lithography simulators, such as, Depict 3.0 cannot handle a large layout in a single simulation run. Also as the layout area to be simulated increases, the simulation time increases by a large amount. So, the Integrated CAD Framework detects the "critical features" from a larger layout, and prepares the input for Depict for the critical feature and some surrounding area only, instead of the whole layout. In this way, two goals are achieved. First, the entire layout is not simulated, thus saving a lot of time. Second, "critical features" in different contexts, depending on other features in the surrounding area, can be identified quickly.

2) Process Simulation: There are several process simulators available, each of which model different parts of the IC fabrication process. SPLAT [14], SAMPLE-3D [15], PROLITH [16], FAIM [17], and Depict [7] are some of the commonly used optical projection lithography simulators. The Integrated CAD Framework uses Depict 3.0. Depict belongs to a suite of process simulators from TMA. Once the layout editor, Magic, is integrated with Depict, it can also be extended to the other tools from TMA which will lead to other process optimizations. Fig. 1 shows a typical lithography simulation flow.

3) Analysis of the Simulation Output: The Integrated CAD Framework analyzes the simulator output to determine an acceptance criteria for the mask considering the specified set of process parameters. It uses Depict to calculate the aerial intensity image of the mask and also to simulate

exposure and development of the photoresist. The Integrated CAD Framework compares the image of the mask after photolithographic simulation to the original mask using pattern matching techniques [18], [19]. It uses the "degree of match" between these to determine acceptability of the mask under current process conditions. This issue is discussed in detail in Section II-B.

In this paper, we try to separate the three steps required to handle "critical features"—1) quick detection of the "critical features" during the conventional design rule checking process; 2) an analysis of the detected "critical features" if the designer so desires; and 3) corrections based on the analysis. This separation is done with the aim of detecting the "critical features" as quickly as possible as well as giving the designer or process engineer the option of taking a closer look at the "critical features" by providing an analysis of the "critical features" based on specified process conditions. This type of analysis can be used to evaluate the limits of any new process technique (such as, phase shifting, off-axis illuminations and others) by evaluating the "critical feature" and their surrounding areas in the layout, under the new process conditions.

4) Application of Proposed Methods to Yield Improvement: Several design techniques have been proposed for many stages of design development and synthesis for yield enhancement [20], [21]. IC device parameters are very sensitive to unavoidable variations in the manufacturing process parameters. Yield degradation due to these global process variations causing line registration errors is known as parametric yield. In [10], the manufacturing yield has been expressed as a product of the probabilities that the analyzed IC does not contain shorts and breaks caused by point defects and line registration errors. Hence, a reduction of line registration errors is directly related to improved yield.

The proposed technique may be contrasted with some existing tools developed for yield analysis of certain types of defects, such as, VLASIC [22], YMAP [23], and [9]. VLASIC is a Monte Carlo simulator that uses defect models and statistics to place random catastrophic point defects on a chip layout and determine what circuit faults, if any, have occurred. This circuit fault information is used to predict yield and optimize design rules. In [9], the authors describe a system that computes "multilayer critical areas" for a range of defect sizes using a deterministic algorithm. This paper models defects as square shaped objects and captures the effect of such a defect on several layers. YMAP [23] is another tool that deterministically calculates the "defect-sensitivity" and "critical area" of a given layout. The goal of such tools is to estimate the yield of a given layout based on an estimation of faults and "critical area," in the presence of random point defects.

On the other hand, this paper defines a method for improving the parametric yield using a technique to avoid line registration errors that arise when a particular "critical feature" gets printed under certain process conditions. Unlike the yield analysis tools mentioned above, the proposed method seeks to bring about a closer interaction between layout design and process simulation, in order to avoid line registration errors during lithography. The proposed method of identifying "critical features" and "printability" analysis will enable the designer or process engineer to take a *closer look* at certain areas in the layout which are potential sources of problems and make sure that those areas will print correctly, without any defects related to the process itself. Hence, this technique may be used in the mask house, as a postprocessor to improve the printing capability of a given mask, specially for applications like DRAM cell design where high level of compaction is the goal.

C. Related Work

Depict 4.0 from TMA [24] is a photolithography simulator that lets the user analyze the printability of regions of an integrated circuit design by simulation of its aerial image and comparison with the original mask design. The nature of the analysis of the printability of a region in Depict 4.0, is very similar to the evaluation of the "critical features" in the Integrated CAD Framework.

However, Depict 4.0 does not automatically identify "critical features" in a layout. Instead, it relies on the user to define the areas of interest which need to be analyzed. The automatic identification of the "critical features" in the Integrated CAD Framework is an extremely important step in printability analysis, especially for large layouts.

Also, Depict 4.0 can be easily integrated into the CAD Framework. As the identification and evaluation of "critical features" in a layout are done in two separate steps in the Integrated CAD Framework (refer to Section II), the CAD Framework can be used to identify the "critical features" and Depict 4.0 can then be used for printability analysis.

II. Implementation

The basic approach followed by the Integrated CAD Framework is as follows.

A. Filter Module

1) Detecting the "Critical Features": The CIF (Caltech Intermediate Format), GDS-II or Magic layout database is passed through a Filter program which identifies the "critical features" in the layout. The current implementation of the Filter module (Fig. 2), identifies the following "critical features": "nested elbows" and "open ends."

The Magic technology specification file contains Conditional Design Rules to detect the "critical features." These new rules are similar to the standard Magic *Edge-based design rules* [25]. The CDRC (Conditional Design Rules Checker) block identifies "critical features" based on these conditional rules following exactly the same algorithm as Magic uses for conventional design rule checking. The CDRC rules are specified in such a way that the "open ends" identified as "critical features" are only as wide as the minimum width allowed by the technology specifications for that layer. Also,

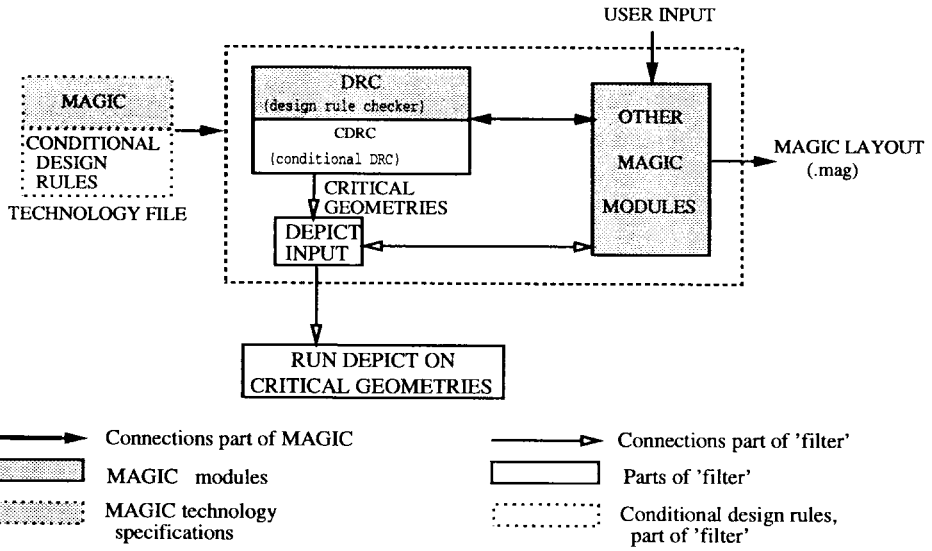

Fig. 2. Integration of the filter module with Magic.

TABLE I
THE PARTS OF AN EDGE BASED RULE

Parameters	Meaning
type1	Material on first side of edge
type2	Material on second side of edge
d	Distance to check on second side of edge
allowed types	List of layers that are permitted within d units on second side of edge
corner types	List of layers in the top-left corner of the edge
corner extension	Amount to extend constraint area when corner types match
error	Error message to be printed if this rule is violated
plane	Plane on which to check the constraints (Defaults to plane of type1 and type2)

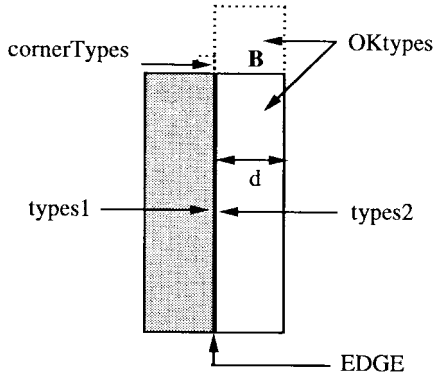

Fig. 3. Application of an edge based rule.

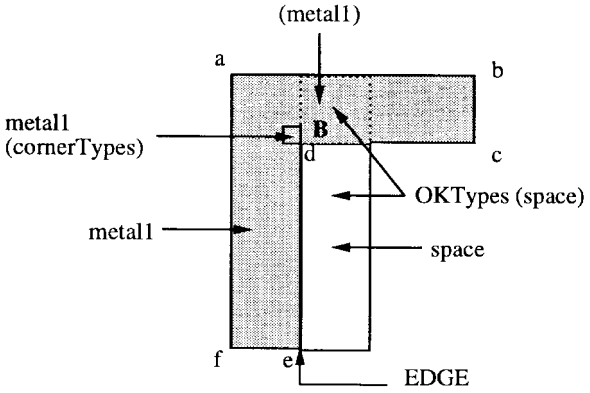

Fig. 4. Application of the rule to detect an elbow.

the "nested elbows" should be spaced by the minimum spacing distance for that layer, in order to be identified as a "critical feature". This is because, any extra margin in terms of width (for both "nested elbows" and "open ends") or spacing between features (for "nested elbows"), will alleviate the problem of corner rounding described before. As an example, identification of nested elbows by the CDRC block is explained below.

Magic *Edge-based rules* have the parts shown in Table I.

Table I is interpreted as follows: whenever an edge has a *type1* layer on its left and *type2* layer on its right, and the corner (shown in Fig. 3) has a *corner types* layer, this rule imposes the restriction that the area on the top right hand corner of the edge can only have an *allowed types* layer. Here, *types* refer to different layers.

The identification of an elbow using the design rule checker is explained in Fig. 4. Whenever an edge has a metal1(m1) layer on its left and space on its right, and the *corner type* is metal1, then area B is checked to see if it is space (*allowed type*). If not, i.e. if area B has metal1, it can be concluded that the structure a-b-c-d-e-f is an elbow.

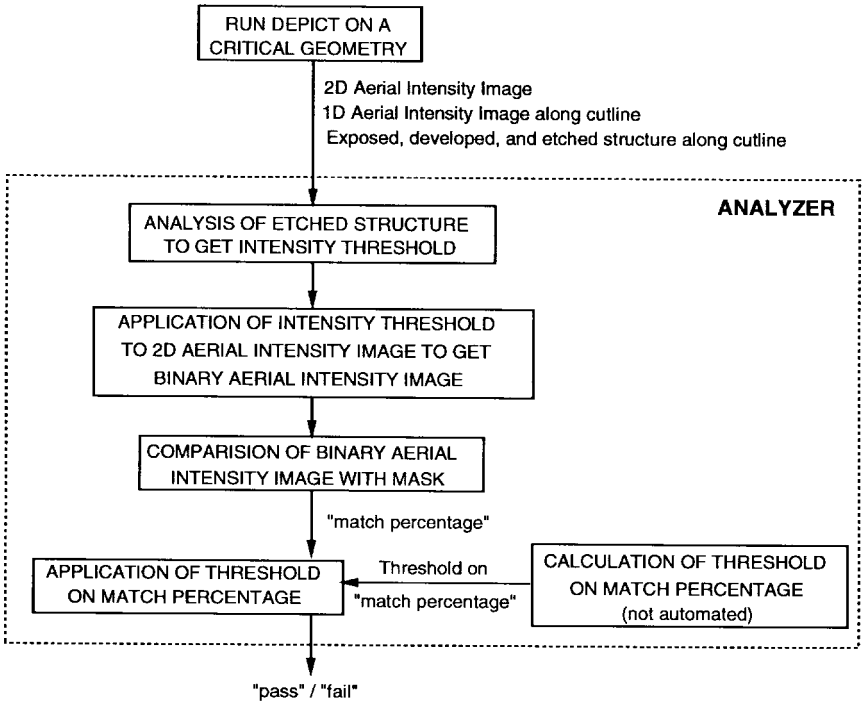

Fig. 5. The Analyzer module.

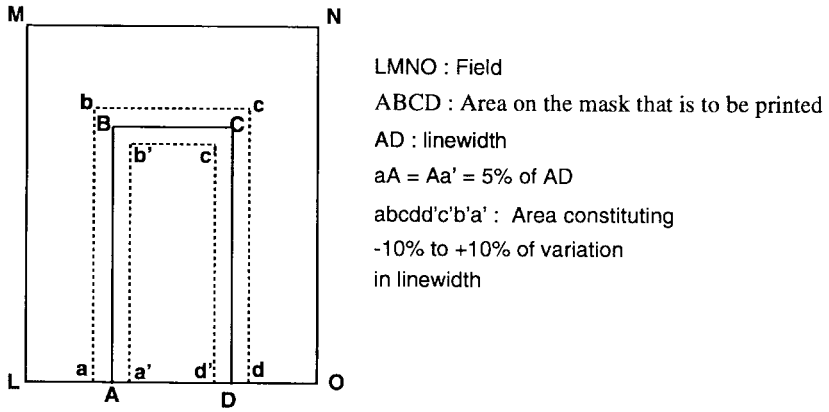

Fig. 6. Determination of threshold on "match percentage": Algorithm 1.

The CDRC block next checks for the presence of another elbow in the vicinity (within a minimum distance). If it finds another, it knows that a pair of nested elbows have been found.

Magic's design rule checker has the limitation of being able to express constraints that depend upon a limited amount of local context. However, Magic represents layout using *corner stitching*—that is, each tile in the Magic representation of the layout has pointers to tiles adjacent to it. Hence, once an elbow is detected, it is possible to check neighboring tiles to see if another elbow exists in the vicinity.

2) Invoking the Filter: The Filter module is invoked from Magic using the design rule checking command of Magic or as a part of Magic's continuous background design rule checker. If a "critical feature" is found, Magic places a label at the point where the "critical feature" is detected. The new label contains the coordinates of the point and the cell name.

3) Running Depict: The layout for the "critical feature" is then automatically converted to Depict input format using the new *depict input* module, which has been added to Magic. Input for Depict for any part of the layout can also be created using a new command that has been added to Magic. This option can be used if the designer feels that a certain portion of the layout needs to be simulated using Depict, even though it is not marked by the Filter as a "critical feature". Depict can then be run from within Magic using another new command.

B. Analyzer Module

The Analyzer module evaluates the simulator outputs (using pattern matching techniques) and decides whether the printed layout will match the designed mask for a particular set of process parameters. Fig. 5 shows the various steps that take place within the Analyzer, for each "critical feature," that the

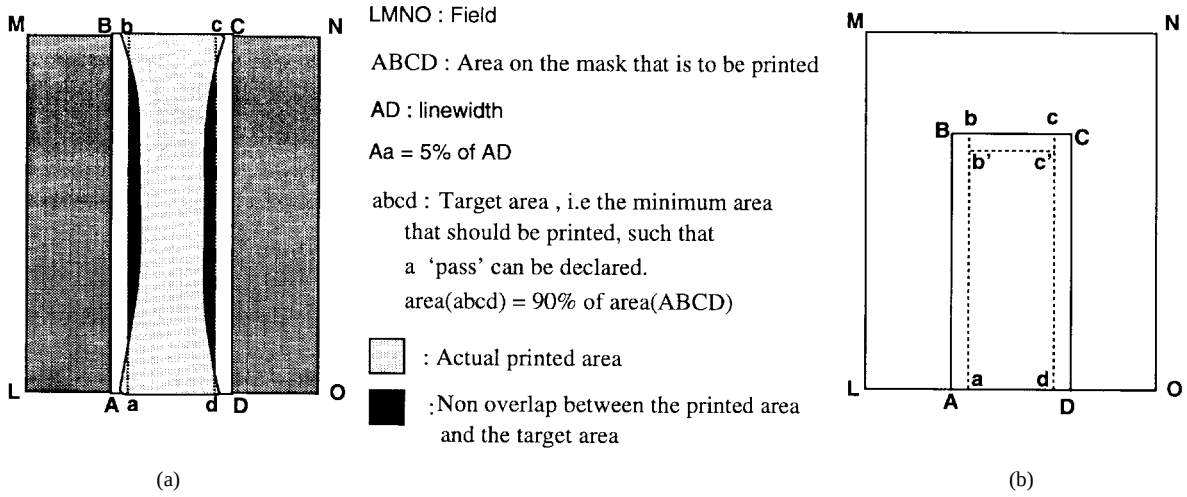

Fig. 7. Determination of "match percentage": Algorithm 2.

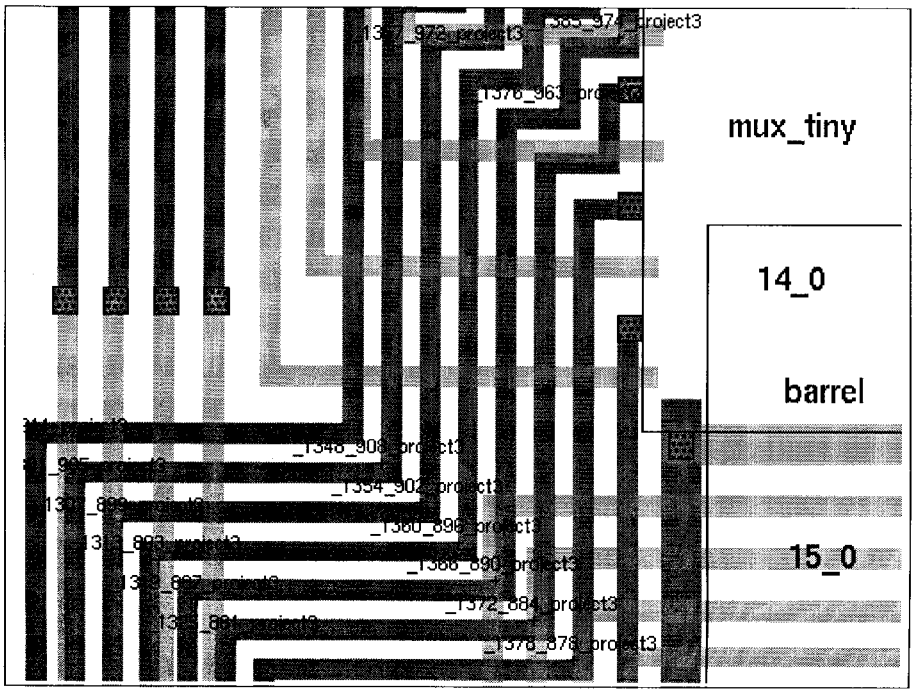

Fig. 8. The layout (routing) evaluated by the framework.

user asks to be analyzed. The following process simulations are done on the 'critical features':

1) Simulation Using Depict: A two-dimensional (2-D) aerial intensity image of the mask is generated. A one-dimensional (1-D) aerial intensity image of the mask is generated along a partial cutline through the 2-D mask. The photoresist structure along the same cutline is exposed, developed and etched for specified process parameters.

This step can be better understood by referring to Fig. 10. Fig. 10(a) shows the 2-D aerial intensity, which is a two dimensional plot of the aerial intensity image of the entire "critical area" that is being analyzed. One-dimensional intensity is the plot of the intensity of the radiation at the wafer versus distance along the cutline labeled as AA′ in Fig. 10(a). The 1-D intensity plot is seen in Fig. 10(b). The photoresist structure along the cutline AA′ in Fig. 10(a) is exposed, developed and etched for specified process parameters. This etched structure can be seen in Fig. 10(c).

2) Binary Aerial Intensity and Binary Mask: The etched structure is analyzed to determine the intensity ("threshold intensity") up to which successful printing occurs. The "threshold intensity" is calculated in two steps as follows.

1) The etched structure is analyzed to calculate the width of the cleared photoresist (for positive photoresist) or the remaining photoresist (for negative resists) across a single line.
2) This width is used along with the 1-D aerial intensity image across the same line to determine the minimum intensity value over the clear region, which is the "threshold intensity."

Again, referring to Fig. 10, the calculation of the "threshold intensity" may be viewed as follows—the profile of the etched structure [Fig. 10(c)] is placed over the 1-D intensity plot along the same cutline AA′ [Fig. 10(b)] to determine the minimum intensity value across the width of the printed line. Thus the "threshold intensity" is the minimum intensity value at the wafer which will result in a print.

This threshold is applied to the 2-D aerial intensity image [Fig. 10(a)] to get the binary aerial intensity image. All points on the 2-D aerial intensity image that have an intensity value above the threshold are marked "1" and those below are marked "0." The resulting binary aerial intensity image can be seen in Fig. 10(d). Also, a binary image of the mask is obtained [Fig. 10(e)] by marking all points inside the mask elements as "1" and all points outside as "0." The binary aerial intensity and the binary mask are then compared to find a percentage of match between the two. If the "match percentage" is above a threshold, the Analyzer declares that the mask "passes" the analysis.

The designer can make some corrections to the original layout based upon this analysis, and the above steps can be repeated until the simulator and the designer find that the layout is acceptable.

3) Determination of "Match Percentage": The Analyzer assumes that a 10% variation in linewidth may be allowed due to inaccuracies in the photolithography process. Ideally, the matching algorithm should perform a "walk" along the center of each printed (simulated) feature, and mark it as "pass" only if the linewidth of the feature is not less than 90% of the desired linewidth, along its entire length. However, this sort of an analysis would be extremely computation intensive, requiring more than one access of each element in the matrix containing the binary aerial intensity image and the binary mask. So, the matching algorithms have been simplified with the aim that the matching routines should access each element of these two matrices only once, but at the same time the loss in accuracy is minimized.

Algorithm 1: Exclusive-or over the entire area

1) A simple exclusive-or is performed between the binary aerial intensity image and the binary mask to determine the "match percentage." Depict calculates the aerial intensity image at 2500 grid points on the mask. Let x be the number of grid points at which the value of the binary aerial intensity image and the binary mask are the same. The amount of agreement can be calculated as: the *match percentage* $= (x/2500) * 100\%$.
2) The determination of threshold on the "match percentage" is explained with the help of Fig. 6 (not drawn to scale). A-B-C-D is the area on the mask that is to be printed, and a-b-c-d-d′-c′-b′-a′ is the area which constitutes a 10% variation in linewidth. Hence, when performing the exclusive-or in the previous step, one can ignore the area a-b-c-d-d′-c′-b′-a′. That is, if there is a match between the binary aerial intensity image and the binary mask at every grid point within L-M-N-O except in the area a-b-c-d-d′-c′-b′-a′, the analysis can result in a "pass". Hence, the "threshold that should be applied to the match percentage" to determine a "pass" or "fail" is calculated as

$$((area(LMNO) - area(abcdd'c'b'a')) / area(LMNO)) * 100\%.$$

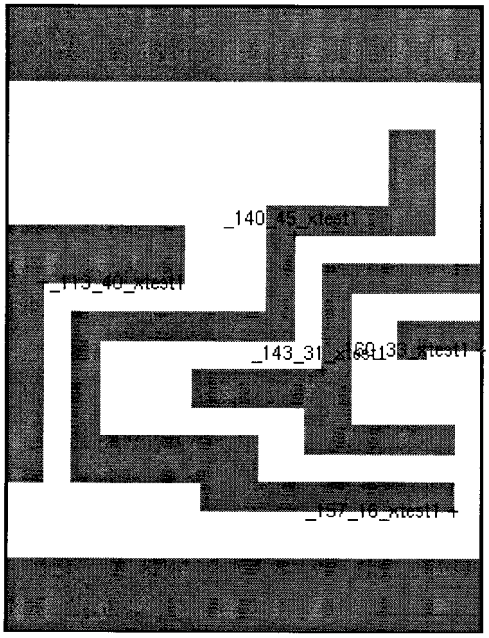

Fig. 9. The layout (part of the metal layer from a D flip-flop cell) evaluated by the framework.

Algorithm 2: A matching algorithm allowing a 10% variation in linewidth

1) The binary mask is converted to a "new" binary mask by shrinking the width of each line by 10%. For each rectangle [A-B-C-D in Fig. 7(a) (not drawn to scale)], in the critical area, the new binary mask is constructed by shrinking rectangle A-B-C-D to rectangle a-b-c-d, such that the width of the rectangle a-b-c-d is 90% of the actual feature A-B-C-D.
2) An exclusive-or is performed between the binary aerial intensity image and this new binary mask. This exclusive-or yields the "match percentage."
3) The "match percentage," as calculated in the previous step, should be 100%, for a critical area to pass this analysis. This is because while matching the binary aerial intensity with the original mask, a 10% variation in linewidth was allowed. However, there is a small inaccuracy in calculating the "match percentage," which will slightly lower the "match percentage" value which a critical area must attain in order to "pass." This inaccuracy is discussed in the next step.
4) The Analyzer determines whether a rectangle ends within a critical area. If a rectangle ends within a critical area, [for example, the open end shown in Fig. 7(a) (not drawn to scale)], a 10% allowance in linewidth variation would imply that we can also ignore the area b-c-c′-b′ [Fig. 7(b)], while performing the exclusive-or. Hence,

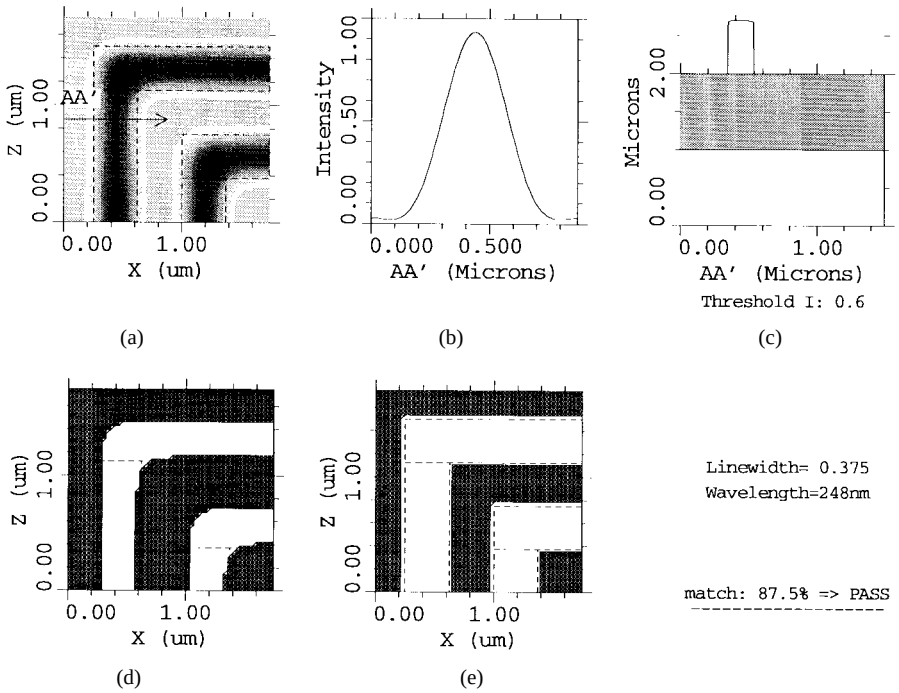

Fig. 10. Output from the analyzer for *linewidth* $= 0.375\ \mu$.

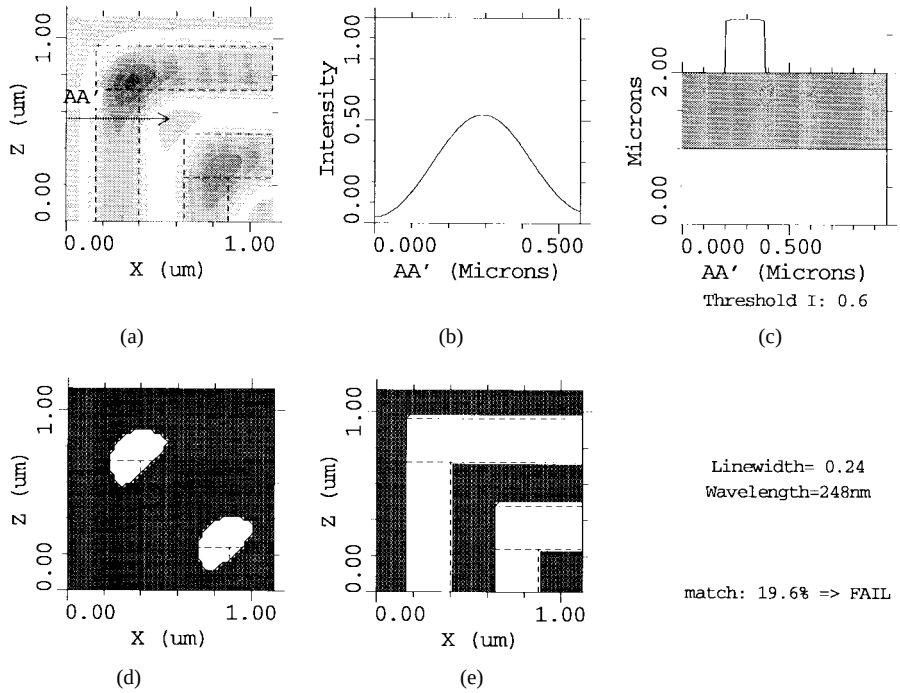

Fig. 11. Output from the analyzer for *linewidth* $= 0.24\ \mu$.

the "threshold on the match percentage" to determine a "pass" is calculated as

$$((area(abcd) - area(bcc'b'))/area(abcd)) * 100\%.$$

Algorithm 2 is more accurate in determining "pass" or "fail" than Algorithm 1, as the matching in Algorithm 2 is almost the same as performing a "walk" down the center of each feature to determine whether there is a 10% variation in linewidth. However, Algorithm 2 requires more computation to determine exactly where it needs to perform the exclusive-or, whereas Algorithm 1 simply performs an exclusive-or of the entire area.

It should be noted here, that, the Analyzer performs the printability analysis, with the assumption that a *perfect* mask is available according to the layout design. It does not attempt to estimate the effect of any unpredicatable defects in a mask like those caused by opaque particles gathered on the surface of the mask [10]. The two algorithms for determination of "match percentages" would fail to estimate the effect of such

TABLE II
RESULTS OF THE EVALUATION OF ELBOWS UNDER DUV CONDITIONS

Linewidth(μ)	Match(%)	Result
0.37	87.5	PASS
0.30	73.6	FAIL
0.24	19.6	FAIL

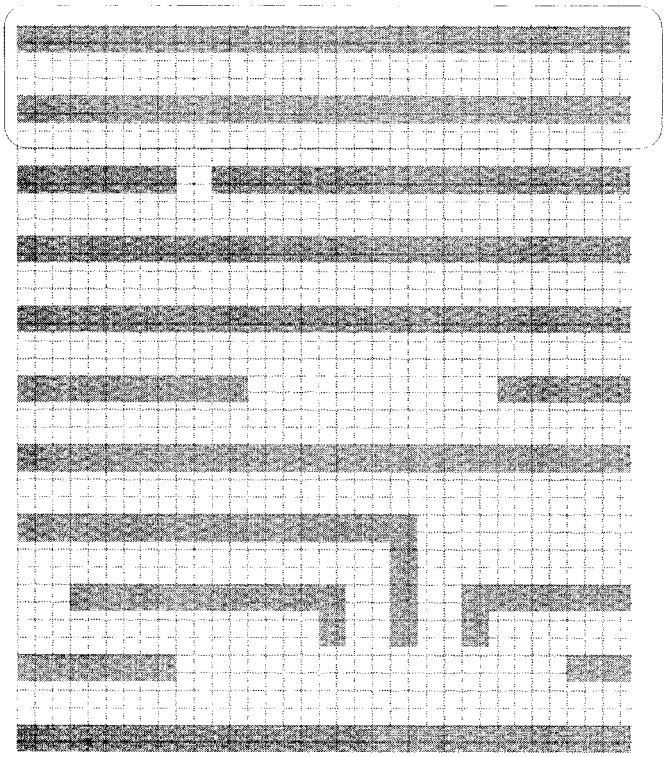

Fig. 12. The original layout: Area: $10.37\ \mu$m $\times$ $8.62\ \mu$m. Linewidth: $0.75\ \mu$m.

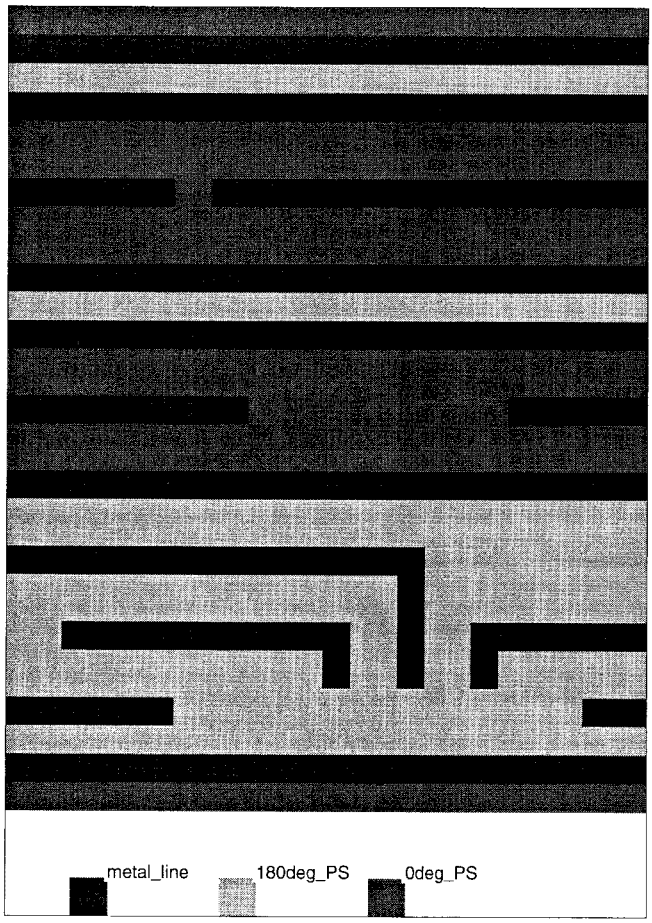

Fig. 13. The compacted layout with phase shifted elements: Area: $9.87\ \mu$m $\times$ $8.62\ \mu$m, Compaction: 5%.

random and isolated defects. However, the CAD Framework uses aerial image simulations of critical features, where the nature of the problems can be predicted (such as, rounding of elbows or shortening of open ends). The applicability of the two algorithms discussed above depends on the predictability of the lithography related problems involving the "critical features."

C. Future Work

The current implementation described in this paper identifies only "nested elbows" and "open ends." An obvious improvement in a future implementation would be to identify other types of "critical features," such as, "closely spaced parallel lines" and "arrays of contact holes." Another improvement would be to reduce some of the burden on the designer that the current implementation places, in terms of choosing which of the identified "critical features" should be analyzed. This can be easily modified, because each "critical feature" found is classified according to the type of geometry (e.g., nested elbows, open ends, etc.) and it is possible to analyze one occurrence of each class. At the same time all occurrence of each class can be automatically tracked through a "critical feature" database. This database could be configured to assist in automating the modification of multiple occurrences of the same class of "critical feature," depending upon other features in the surrounding area, if the "printability" analysis indicates a high possibility of failure.

In the next step, any proximity effects correction tool [26]–[29], can be used for optical proximity corrections (OPC), if a certain layout fails the "printability" analysis. OPC are corrections to the layout in the form of relocating existing features or adding sub-resolution serifs as discussed in [12]. Addition of such a step will be aimed toward hiding the entire "critical features" filtering-analysis-corrections loop from the layout designer unless the designer specifically wants to look at a particular process simulation.

III. RESULTS

This section demonstrates the various features of the Integrated CAD Framework, namely (A) Identification of "critical features" in a layout and, (B) evaluation of a specific "critical feature."

A. Identification of "Critical Features"

In this section, the Integrated CAD Framework automatically identifies "critical features" in two pieces of layout.

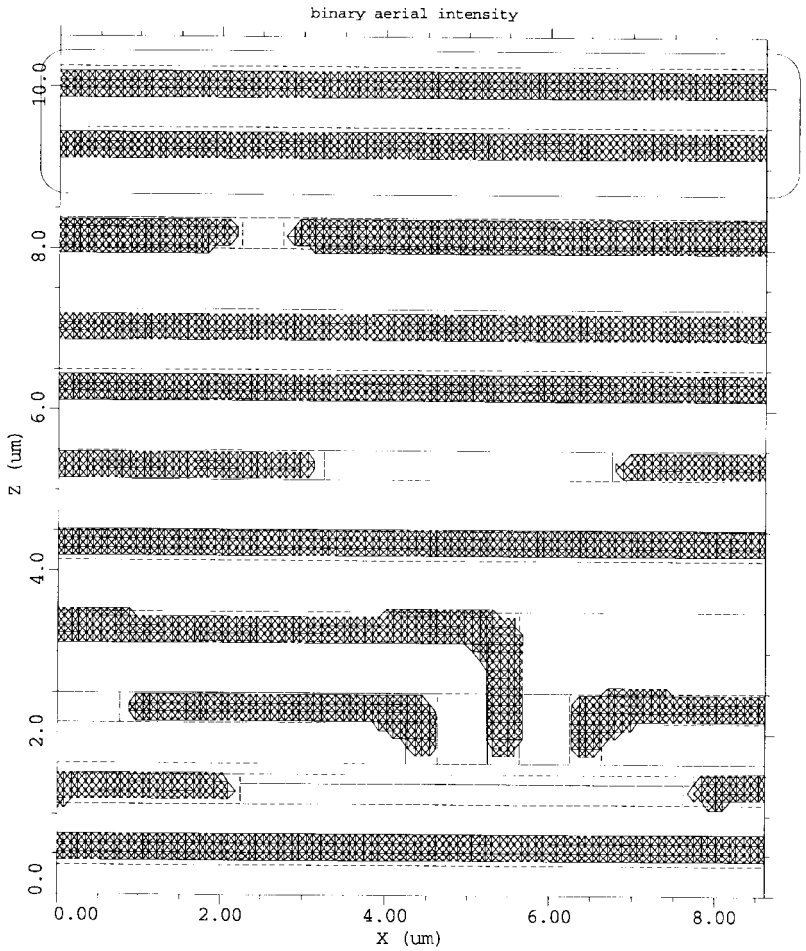

Fig. 14. Binary aerial intensity image for the compacted layout with phase shifting: Threshold: 0.4, Match: 90% $=>$ PASS.

Fig. 8 shows a Magic layout that is a part of the routing from a larger layout of an Arithmetic Logic Unit. The placement of the subcells and the connections between them necessitate the use of nested elbows in the routing.

The labels mark some of the "nested elbows" automatically identified by the Integrated CAD Framework, in this piece of layout. The name of a label contains the coordinates of the point in the layout that it marks and the name of the cell. Each pair of nested elbows are marked separately, so that input for Depict 3.0 may be generated for any pair. Thus Depict 3.0 will have to simulate only a small area of the layout. It may be noted, that Fig. 8 does not show the labels for all the critical features found by the tool—some have been deleted to retain readability.

Fig. 9 shows another piece of Magic layout from the metal layer of a D flip-flop cell from the standard cell library in the Lager suite of CAD software [30]. The Integrated CAD Framework identifies two pairs of "open ends" and three occurrences of closely spaced "nested elbows" in the piece of layout shown in the figure. It may be noted that the layout also contains wider "open ends" as well as wider and more widely spaced "nested elbows" that are not tagged as "critical features" as discussed in Section II-A.

One of the critical areas was chosen for evaluation. The results of the evaluation are presented in the next section.

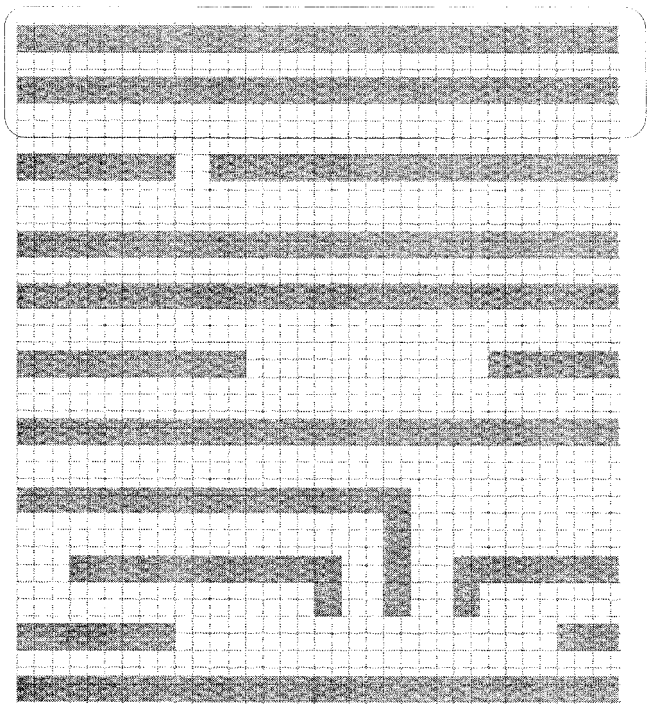

Fig. 15. The compacted layout without phase shifted elements: Area: $9.87\ \mu$m $\times$ $8.62\ \mu$m, Compaction: 5%.

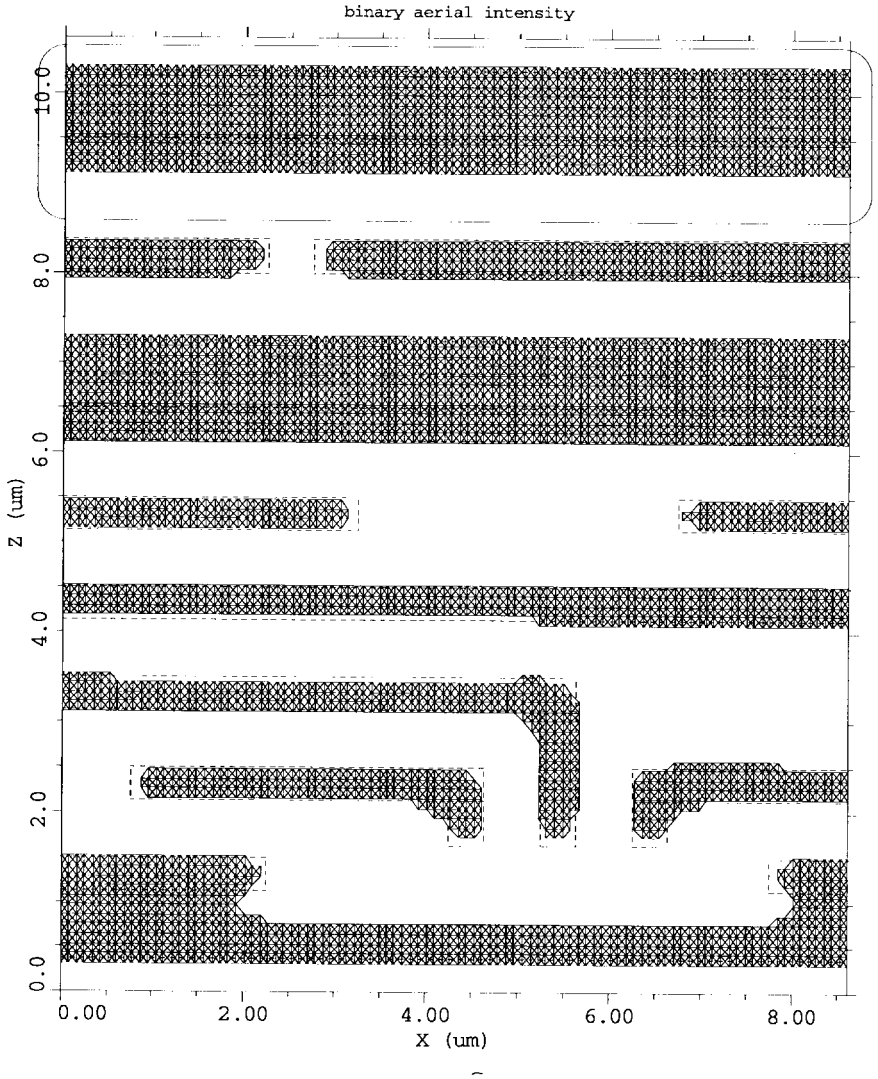

Fig. 16. Binary aerial intensity image for the compacted layout without phase shifted elements: Threshold: 0.4, Match: 80% => FAIL.

B. Evaluation of a Set of Nested Elbows Under DUV Conditions

In this section, a pair of "nested elbows," extracted from a larger layout, is evaluated under deep ultra violet (DUV) lithography conditions for linewidth ranging from 0.37 to 0.25 μm. The modeling of the photoresist (SNR248 from Shipley Co.) as well as the exposure and development of the resist is done explicitly using data obtained from two papers [31], [32], in which, the performance of SNR248 photoresist is evaluated for different values of numerical aperture, defocus, exposure dose, resist thickness, softbake and post exposure bake for a nominal linewidth of 0.35 μm. The optical characteristics of silicon, the SNR248 resist, and an anti-reflective coating, as a function of wavelength (248 nm) were specified to Depict. Also, a model for development of SNR248 based on the Mack model [33] was defined.

The evaluation of the structure for two different linewidths are shown in Figs. 10 and 11. The steps followed during this evaluation has been explained in Section II-B. Fig. 10 shows the analysis for a linewidth of 0.375 μm. Fig. 10(c) shows the exposed and developed structure with a printed line in the center. The width of this line is used with the 1-D aerial intensity image of Fig. 10(b) to find the minimum intensity over the printed line ("threshold intensity"). The "threshold intensity" is reported below Fig. 10(c). The "threshold intensity" is applied to the aerial intensity image in Fig. 10(a) to obtain the binary aerial intensity image in Fig. 10(d). The binary aerial intensity is compared to the original mask [Fig. 10(e)] to determine the "match percentage." The "match percentage" is reported at the bottom of Fig. 10. This analysis pronounces this layout, with a linewidth of 0.375 μm, under the specified process conditions a "pass."

Fig. 11 shows a similar analysis for a linewidth of 0.24 μm. However, in this case the analysis concludes that under the given process conditions, a pair of nested elbows with a linewidth of 0.24 μm, cannot be printed accurately. Hence the analyzer marks it as a "fail." Table II summarizes the results of this experiment.

C. Application of Phase Shifting to a Layout in Order to Achieve Compaction

This section discusses how the printability analysis capability of the Integrated CAD Framework can be used to evaluate a layout under a different process technique (using phase shifting masks).

In a phase-shifted mask, every other element in a closely packed mask contains a phase-shifter. As a result, the light amplitude after passing through the mask varies from 1 to 0 to -1, whereas it varies only from 1 to 0 in a conventional mask. The intensity, which is proportional to the square of the amplitude restores the spatial frequency of the mask openings but with far greater contrast and, therefore, resolution.

The Magic layout editor was modified to support the representation of phase shift masks and was used together with the Analyzer to compact a piece of layout by inserting phase shifted elements into it. The piece of layout, evaluated in this section, was generated automatically by a router in the Lager suite of CAD software [30]. The wire routing which occurs between rows of standard cells is done using two metal layers (metal1 and metal2 in Magic). Metal1 is run in the horizontal direction and metal2 is run in the vertical direction with appropriate contacts between the two layers. The piece of layout extracted for this example, is a part of the metal1 layer of the wire routing. This layout (Fig. 12) has been already optimized by the router to have lines and spaces of width best suited for a transmission mask. Phase shifted parts were added to the layout with the goal that phase shifting will allow closer spacing between the lines. Fig. 13 shows the layout after insertion of the phase shifted elements. The use of the phase shifted elements allow closer spacing between the lines and hence a more compact layout. Fig. 15 shows the same compacted layout with the phase shifted elements removed. In Figs. 12–14, a certain area near the top of the layout has been highlighted to show a region where the use of phase shifted elements has allowed closer spacing between two adjacent lines.

The compacted layout with and without the phase shifted elements was evaluated by the Analyzer. The photoresist used was KODAK820 and the aerial intensity image was obtained with light of wavelength 365 nm (i-line) and a lens of numerical aperture of 0.4. The parameters for the photoresist were taken from the Depict 3.0 library. Fig. 14 shows the binary aerial intensity image with an intensity threshold of 0.4, for the compacted layout with the phase shifted elements. The binary aerial intensity image closely resembles the mask and the Analyzer marks it as a "pass." The same experiment was repeated for the compacted layout without the phase shifted elements. Fig. 16 shows the binary aerial intensity image with an intensity threshold of 0.4, for the compacted layout without the phase shifted elements. The poor quality of the binary aerial intensity image clearly shows that the compacted layout cannot be used as a transmission mask.

Thus the Integrated CAD Framework can be used to build an automatic phase shift mask generator from a mono-layer layout. In this section, phase shifted elements were inserted in a relatively small piece of layout. The same technique can be automated and applied to larger layouts, such as a 1 Giga-bit DRAM, in order to achieve larger percentages of compaction.

IV. Conclusion

A technique for identifying and evaluating "critical features" in a layout has been developed and implemented in the Integrated CAD Framework. The CAD Framework has been built as an extension to existing CAD tools, that is Magic and Depict. The examples in Section III show that the Integrated CAD Framework provides a simple and interactive method of evaluating a layout or a process technique. Hence, our technique has potential for use either to evaluate the limits of any new and nonconventional process technique in an early process definition phase or in a mask house, as a postprocessor to improve the printing capability of a given mask.

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Chaitali Sengupta (S'97) was born in Durgapur, India, on March 19, 1970. She received the B. Tech. degree in computer science and engineering from Indian Institute of Technology, Kharagpur, India, in 1992 and the M.S. degree in electrical engineering from Rice University, Houston, TX, in 1995. She is currently pursuing the Ph.D. degree at Rice University.

In 1992–1993, she was a Software Design Engineer with Texas Instruments, India. Her research interests include VLSI CAD, VLSI design and microlithography, and implementation issues in wireless communication systems.

Joseph R. Cavallaro (S'78–M'82) was born in Philadelphia, PA, on August 22, 1959. He received the B.S. degree from the University of Pennsylvania, Philadelphia, in 1981, the M.S. degree from Princeton University, Princeton, NJ, in 1982, and the Ph.D. degree from Cornell University, Ithaca, NY, in 1988, all in electrical engineering.

From 1981 to 1983, he was with AT&T Bell Laboratories, Holmdel, NJ. In 1988, he joined the faculty of Rice University, Houston, TX, where he is an Associate Professor of Electrical and Computer Engineering. From July 1996 through June 1997, he served at the National Science Foundation as director of the Prototyping Tools and Methodology program in the MIPS division. His research interests include computer arithmetic, fault tolerance, VLSI design and microlithography, and VLSI architectures and algorithms for wireless communication systems and robotics.

Dr. Cavallaro is a recipient of the NSF Research Initiation Award (1989–1992) and is a member of ACM, Tau Beta Pi, and Eta Kappa Nu.

William L. Wilson, Jr. (S'68–M'71–SM'87) was born on February 6, 1943. He received the B.S. degree in 1965, the M.E.E. degree in 1966, and the Ph.D. degree in 1972, all in electrical engineering, from Cornell University, Ithaca, NY.

From 1971 to 1972, he was an Instructor-Research Associate with the Electrical Engineering School at Cornell University. From 1972 to the present, he has been with the Electrical and Computer Engineering Department, Rice University, Houston, TX. He is currently a Professor. His research interests include advanced photolithographic techniques, laser processing of materials, and semiconductor devices.

Dr. Wilson is a member of Tau Beta Pi, Eta Kappa Nu, Sigma Xi, and the American Physical Society.

Frank K. Tittel (SM'72–F'86) was born in Berlin, Germany, in 1933. He received the M.A. and Ph.D. degrees from Oxford University, Oxford, U.K.

From 1959 to 1967, he was a Research Physicist with the General Electric Research and Development Center, Schenectady, NY. Since 1967, he has been with Rice University, Houston, TX, where he is a Professor with the Department of Electrical and Computer Engineering. His primary research interests include laser devices, laser spectroscopy, and laser applications in microlithography and laser medicine.

Dr. Tittel is a Fellow of the Optical Society of America and the American Physical Society, and a member of the IEEE Laser and Electro-Optics Society.